



General Description

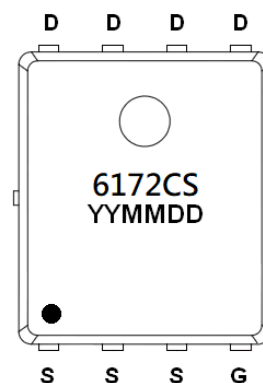
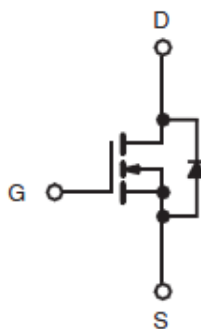
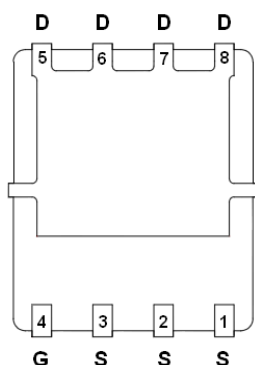
AFN6172CS, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- 100V/20A, $R_{DS(ON)}=4.0m\Omega@V_{GS}=10V$
- 100V/15A, $R_{DS(ON)}=5.0m\Omega@V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- DFN5X6-8L package design

Pin Description (DFN5X6-8L)



Application

- Networking / Telecom / Server
- LED Lighting Applications
- Quick Charger Applications
- DC-DC Primary Side Switch

Pin Define

Pin	Symbol	Description
1~3	S	Source
4	G	Gate
5~8	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN6172CSFN568RG	6172CS	DFN5X6-8L	Tape & Reel	2500 EA

※ 6172CS : Parts Code

※ YYMMDD : Date Code

※ AFN6172CSFN568RG : 13" Tape & Reel ; Pb- Free ; Halogen- Free



Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless otherwise noted)

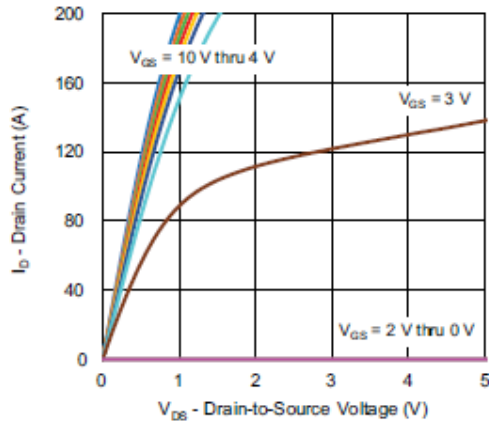
Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate -Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_J=150^\circ\text{C}$)	I_{DSM}	$T_C=25^\circ\text{C}$	100
		$T_C=70^\circ\text{C}$	75
Pulsed Drain Current ($t=100\mu\text{s}$)	I_{DM}	$T_A=25^\circ\text{C}$	23
		$T_A=70^\circ\text{C}$	19
Continuous Source Current (Diode Conduction)	I_S	$T_C=25^\circ\text{C}$	94
		$T_A=25^\circ\text{C}$	5.6
Single Pulse Avalanche Current	I_{AS} E_{AS}	L=0.1mH	35
			62
Power Dissipation	P_D	$T_C=25^\circ\text{C}$	104
		$T_C=75^\circ\text{C}$	66
Operating Junction Temperature	T_J	$T_A=25^\circ\text{C}$	6.25
		$T_A=75^\circ\text{C}$	4.0
Storage Temperature Range	T_{STG}	150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	-55/150	$^\circ\text{C}$
Maximum Junction-to-Case (Drain)	$R_{\theta JA}$	15	$^\circ\text{C/W}$
		Steady-State	1.0

Electrical Characteristics ($T_A=25^\circ\text{C}$ Unless otherwise noted)

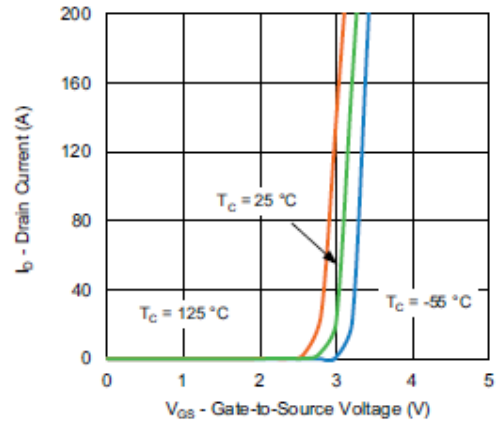
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu\text{A}$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0	1.7	2.5	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$			1	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=85^\circ\text{C}$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 10V, V_{GS}=10V$	40			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		3.5	4.0	m Ω
		$V_{GS}=4.5V, I_D=15A$		4.2	5.0	
Forward Transconductance	g_{FS}	$V_{DS}=15V, I_D=20A$		85		S
Diode Forward Voltage	V_{SD}	$I_S=5A, V_{GS}=0V$		0.75	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=50V, V_{GS}=4.5V$ $I_D=20A$		45	65	nC
Gate-Source Charge	Q_{gs}			18		
Gate-Drain Charge	Q_{gd}			12		
Gate Resistance	R_g	f=1MHz	0.4	1.7	3.0	Ω
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V$ f=1MHz		6000		pF
Output Capacitance	C_{oss}			375		
Reverse Transfer Capacitance	C_{rss}			20		
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, R_L=2.5\Omega$ $I_D=20A, V_{GEN}=10V$ $R_G=1\Omega$		12	25	ns
	t_r			8	15	
Turn-Off Time	$t_{d(off)}$			40	80	
	t_f		10	20		



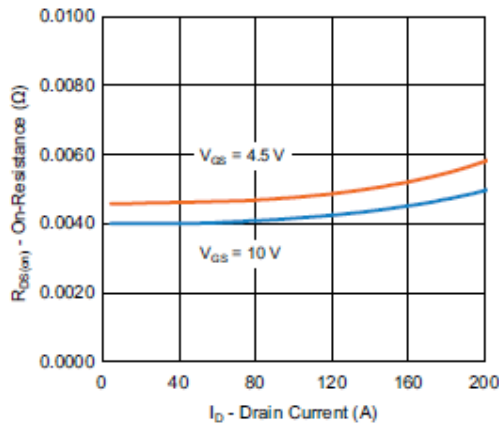
Typical Characteristics



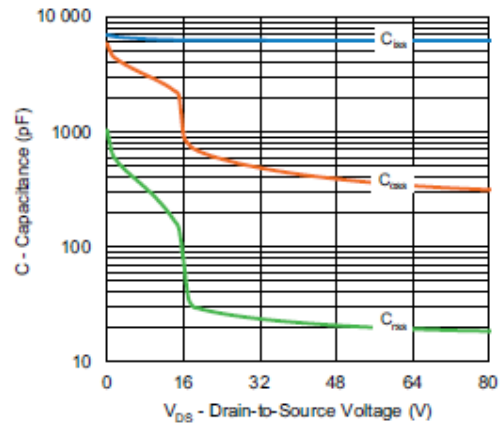
Output Characteristics



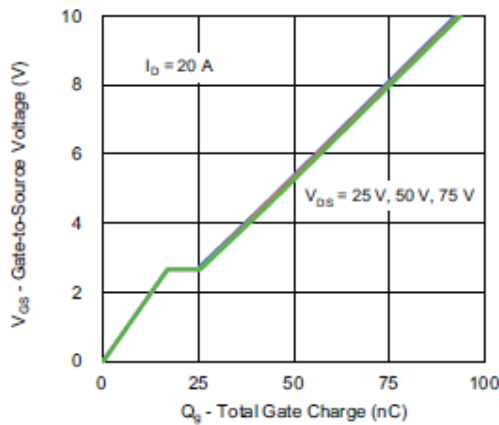
Transfer Characteristics



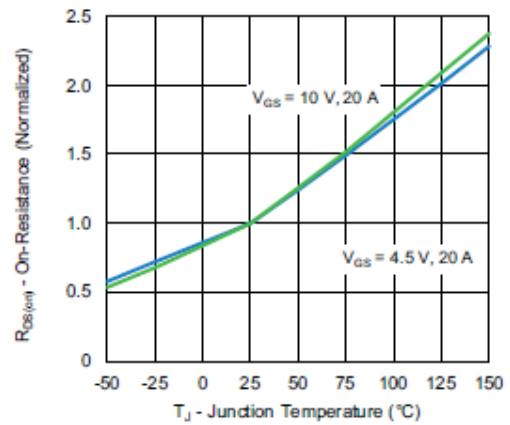
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



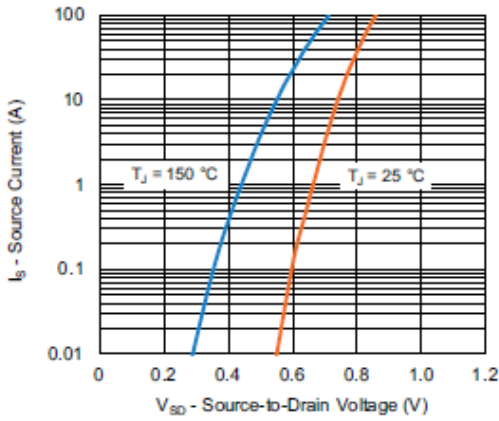
Gate Charge



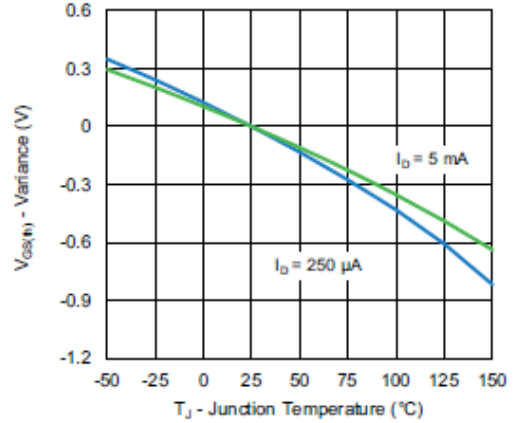
On-Resistance vs. Junction Temperature



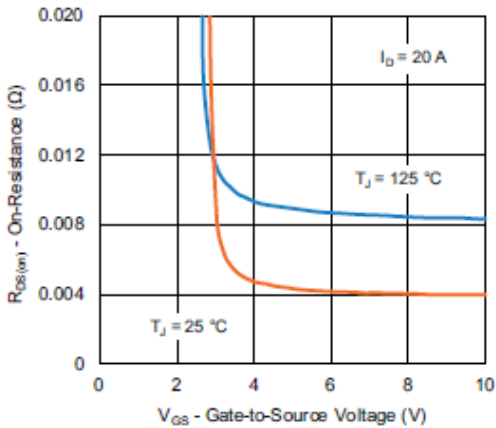
Typical Characteristics



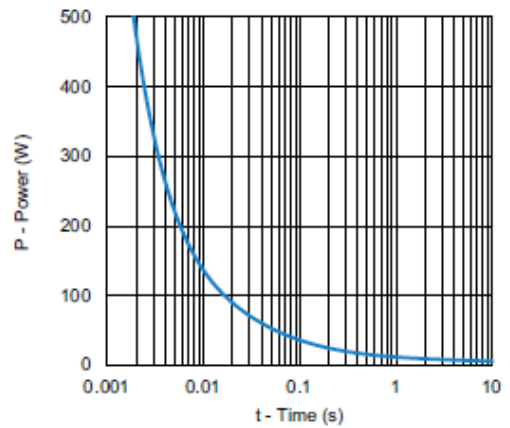
Source-Drain Diode Forward Voltage



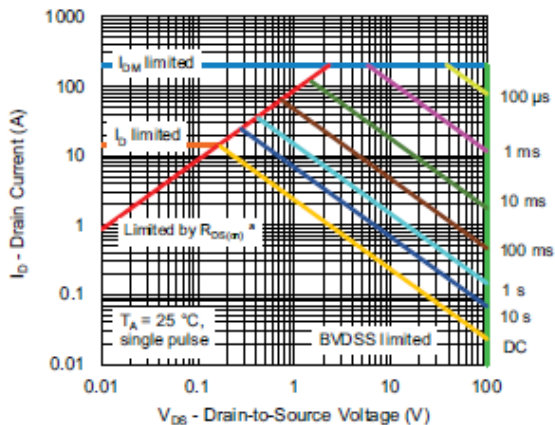
Threshold Voltage



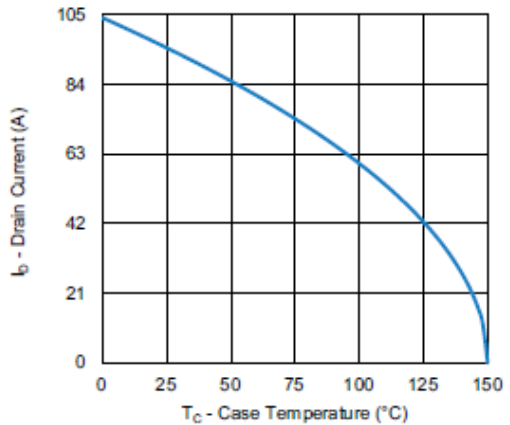
On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



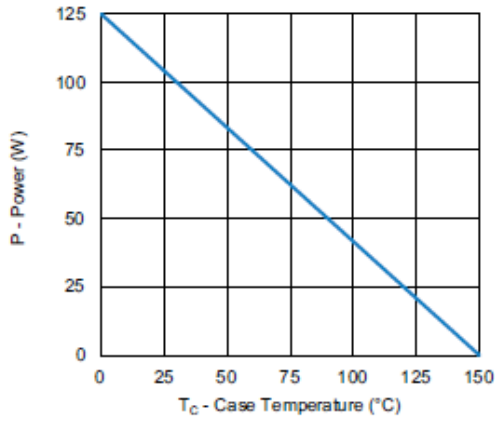
Safe Operating Area, Junction-to-Ambient



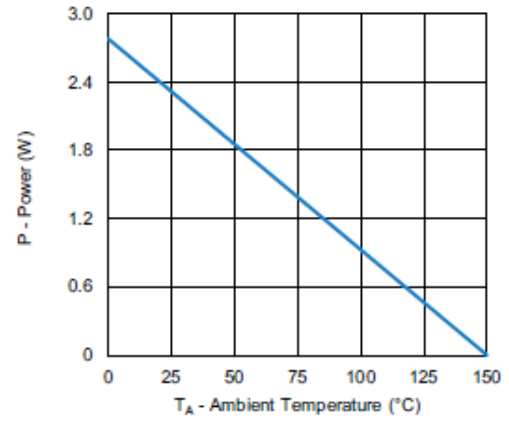
Current Derating^a



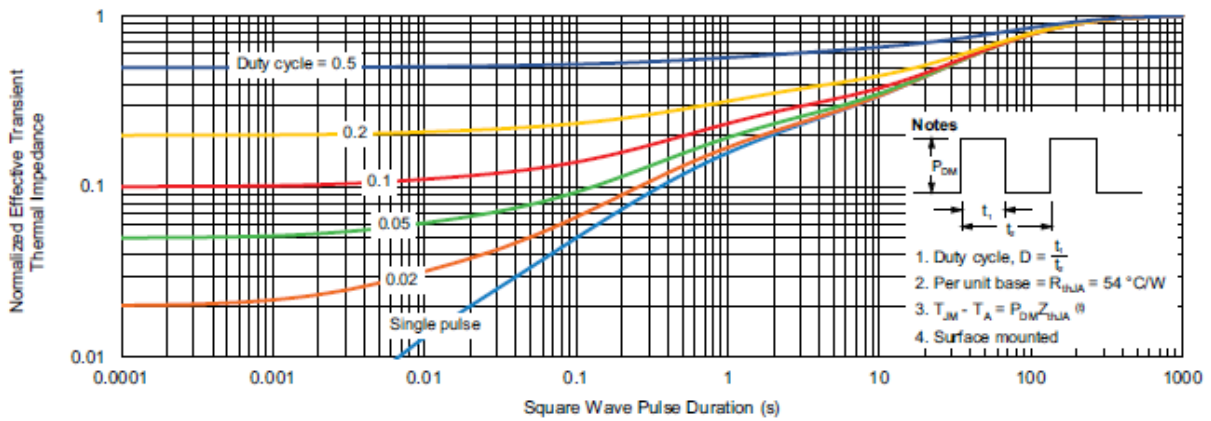
Typical Characteristics



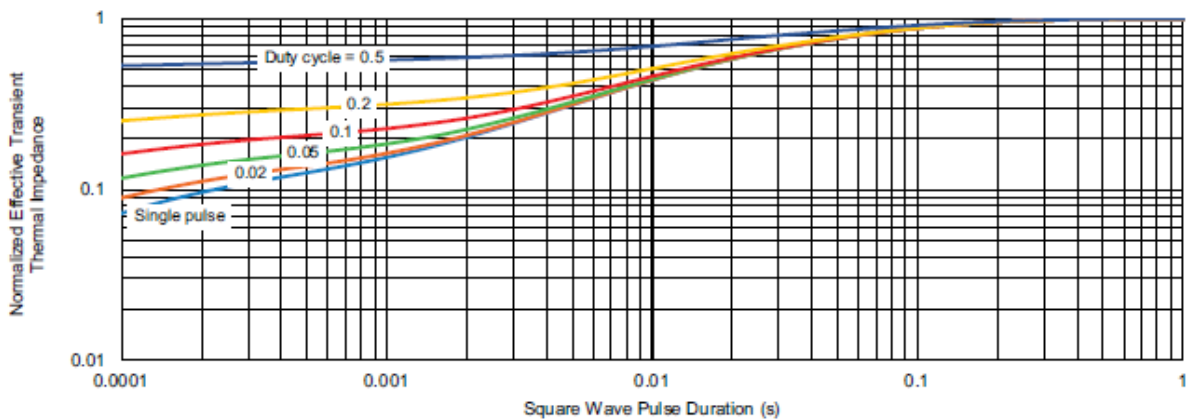
Power, Junction-to-Case



Power, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient

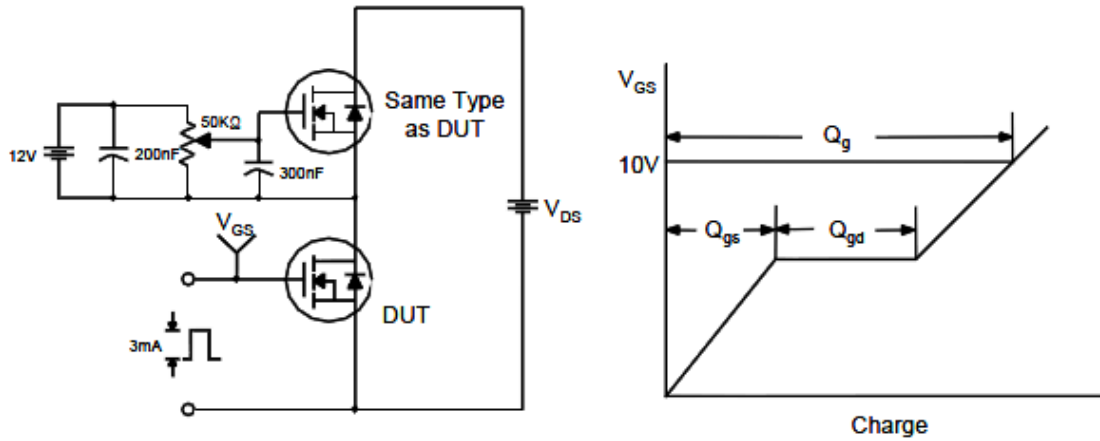


Normalized Thermal Transient Impedance, Junction-to-Case

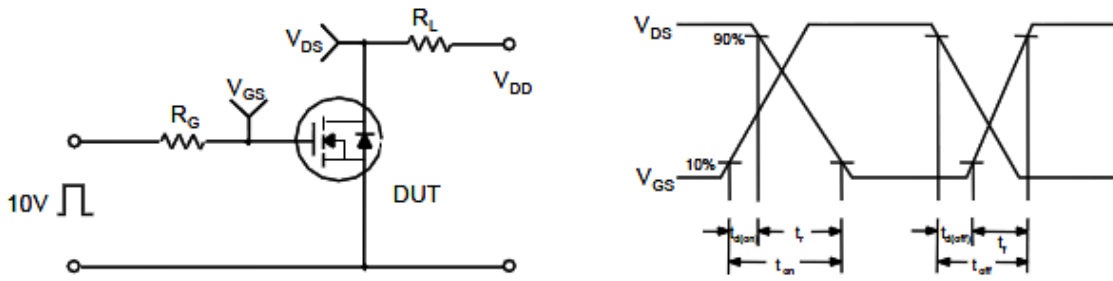


Typical Characteristics

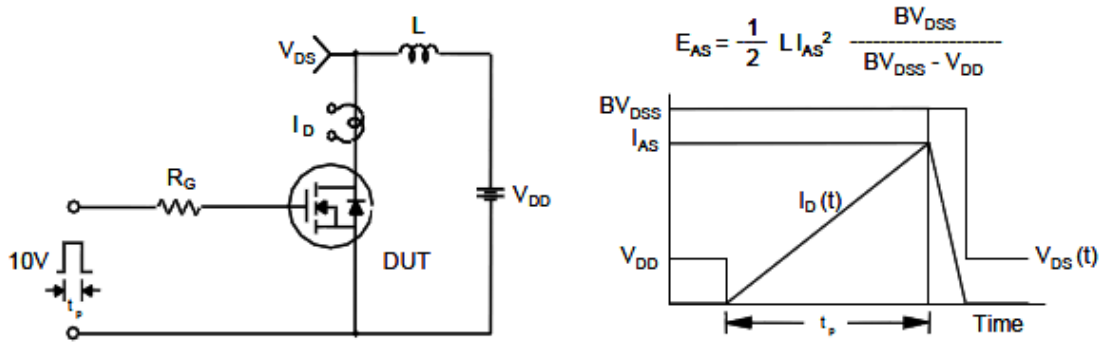
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

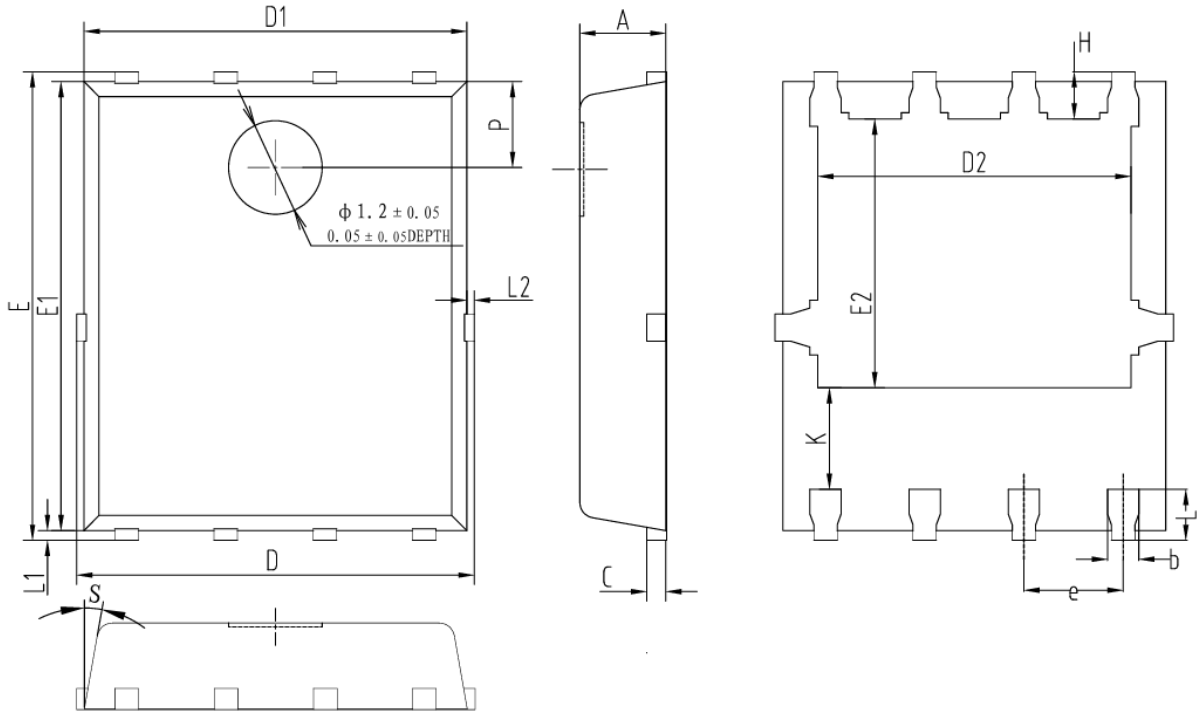


Unclamped Inductive Switching Test Circuit & Waveforms





Package Information (DFN5X6-8L)



COMMON DIMENSIONS (UNIT of MEASURE=MILLIMETER)											
SYMBOL	MIN	NOM	MAX	SYMBOL	MIN	NOM	MAX	SYMBOL	MIN	NOM	MAX
A	1.00	1.10	1.20	e	1.17	1.27	1.37	L	0.55	0.65	0.75
b	0.35	0.40	0.45	E	5.90	6.00	6.10	L1	0	0.10	0.20
c	0.19	0.25	0.30	E1	5.70	5.75	5.80	L2	0	0.10	0.20
D	4.80	5.10	5.20	E2	3.35	3.45	3.55	P	1.00	1.10	1.20
D1	4.80	4.90	5.00	H	0.50	0.60	0.70	S	8°	10°	12°
D2	3.90	4.00	4.10	K	1.20	1.30	1.40				

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