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HXMH65M600ES
N-Channel Power MOSFET

Description

The 650V E series has excellent low on-resistance and gate charge by utilizing charge balance technology .
This technology combines the benefits of an excellent switching performance with ease of usage and robustness. Consequently, the 650V E series is suitable for application requiring superior efficiency and extra safety margin for design with higher voltage.

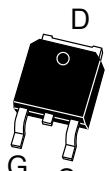
Features

BV_{DSS} @ $T_{J,max}$	I_D	$R_{DS(on),max}$	$Q_{g,typ}$
700 V	6.3 A	600 mΩ	11.9 nC

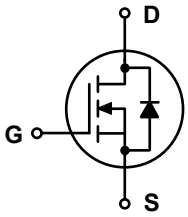
- Reduced Switching & Conduction Losses
- Lower Switching Noise
- 100% Avalanche Tested
- Pb-free, Halogen Free, and RoHS Compliant
- Pb-free and RoHS Compliant
- Compliance with EU REACH

Applications

- PFC, Hard & Soft Switching Topologies
- Industrial & Consumer Power Supplies



TO-252-2L



Absolute Maximum Ratings (T_C = 25℃ unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage		±30	V
I_D	Drain Current	Continuous (T_C = 25℃)	6.3*	A
		Continuous (T_C = 100℃)	4.0*	
I_{DM}	Drain Current	Pulsed (Note1)	28.8*	A
E_{AS}	Single Pulsed Avalanche Energy	(Note2)	22	mJ
I_{AS}	Avalanche Current	(Note2)	1.9	A
E_{AR}	Repetitive Avalanche Energy	(Note1)	0.61	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt	(Note3)	20	
P_D	Power Dissipation	(T_C = 25℃)	69	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	℃
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 10 Seconds		260	℃

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Marking	Package	Packing Method	Quantity
HXMH65M600ES	H65M600ES	TO-252-2L	Reel	3000 units

Electrical Characteristics (T_C = 25℃ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150℃	700			
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V			1	μA
		V_{DS} = 520 V, V_{GS} = 0 V, T_J = 125℃		2		
I_{GSS}	Gate-Source Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 0.5 mA	2.5		4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 2.5 A		511	600	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 250 kHz		402		pF
C_{oss}	Output Capacitance			12		pF
$C_{o(tr)}$	Time Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		160		pF
$C_{o(er)}$	Energy Related Output Capacitance			19		pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 400 V, I_D = 2.5 A, V_{GS} = 10 V		11.9		nC
Q_{gs}	Gate to Source Charge			2.6		nC
Q_{gd}	Gate to Drain “Miller” Charge			5.8		nC
R_G	Gate Resistance	f = 1 MHz		6.5		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 400 V, I_D = 2.5A, V_{GS} = 10 V, R_G = 10 Ω See Figure 13		7		ns
t_r	Turn-On Rise Time			9		ns
$t_{d(off)}$	Turn-Off Delay Time			30		ns
t_f	Turn-Off Fall Time			15		ns
Source-Drain Diode Characteristics						
I_S	Maximum Continuous Diode Forward Current				6.3	A
I_{SM}	Maximum Pulsed Diode Forward Current				18.9	A
V_{SD}	Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 2.5 A			1.2	V
t_{rr}	Reverse Recovery Time	V_{DD} = 400 V, I_{SD} = 2.5 A, dI_F/dt = 100 A/μs		181		ns
Q_{rr}	Reverse Recovery Charge			1.14		μC

※Notes:
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 1.9 A, R_G = 25 Ω, starting T_J = 25℃.
3. I_{SD} ≤ 2.5 A, di/dt ≤ 100 A/μs, V_{DD} ≤ 400 V, starting T_J = 25℃.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

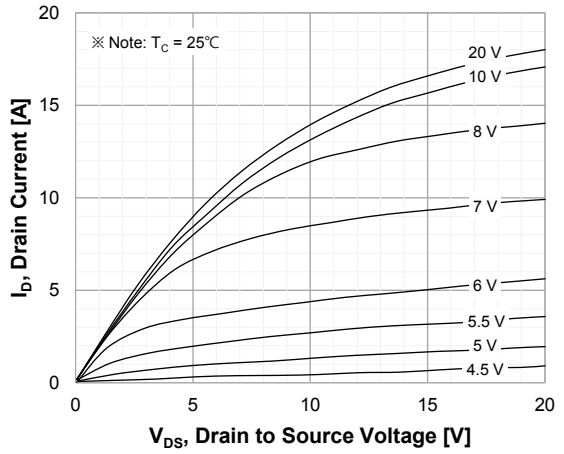


Figure 2. Transfer Characteristics

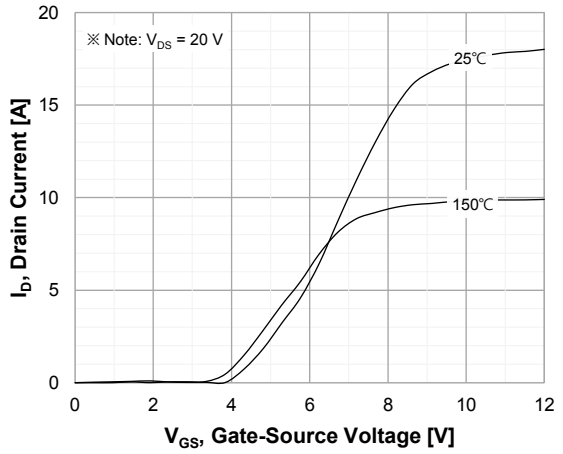


Figure 3. On-Resistance Characteristics vs. Drain Current and Gate Voltage

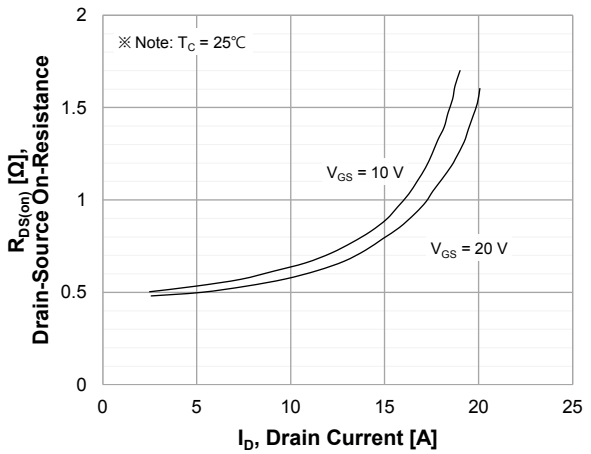


Figure 4. Diode Forward Voltage Characteristics vs. Source-Drain Current and Temperature

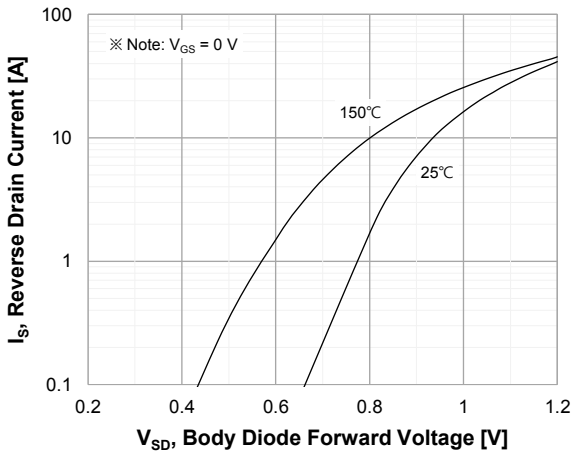


Figure 5. Capacitance Characteristics

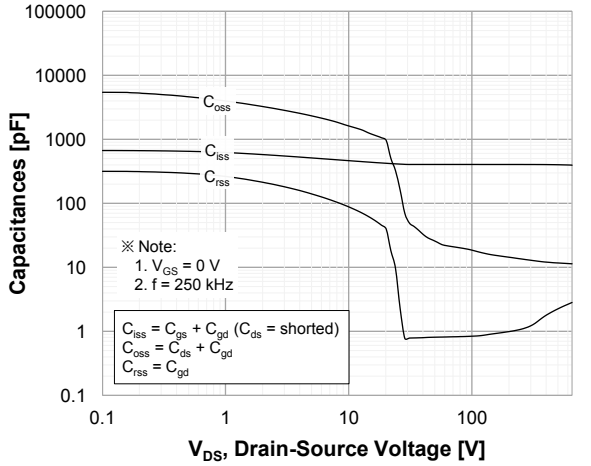
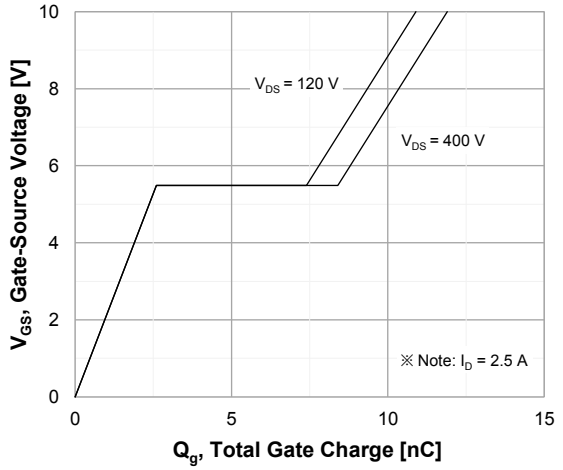


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics

Figure 7. Breakdown Voltage Characteristics vs. Temperature

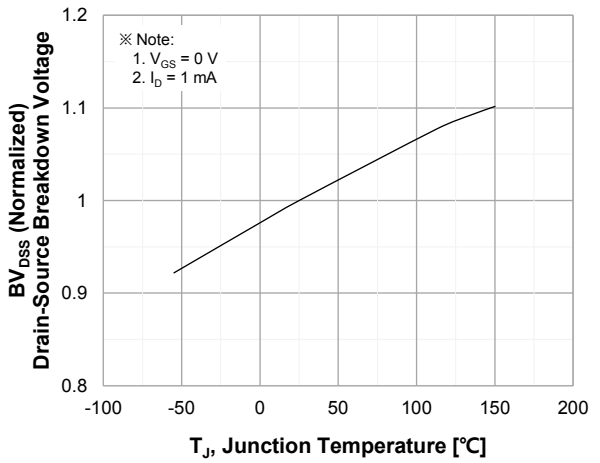


Figure 8. On-Resistance Characteristics vs. Temperature

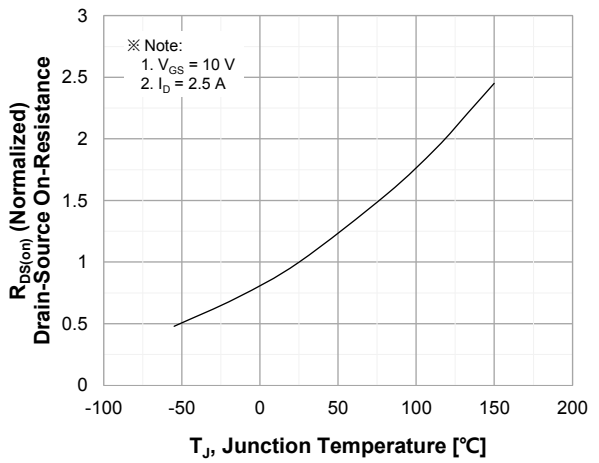


Figure 9. Maximum Safe Operating Area

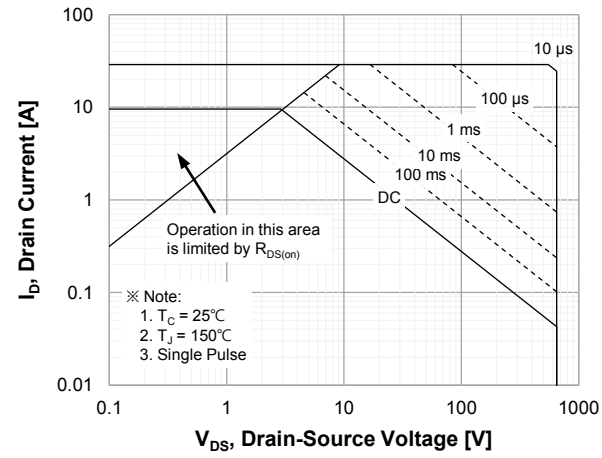


Figure 10. Maximum Drain Current vs. Case Temperature

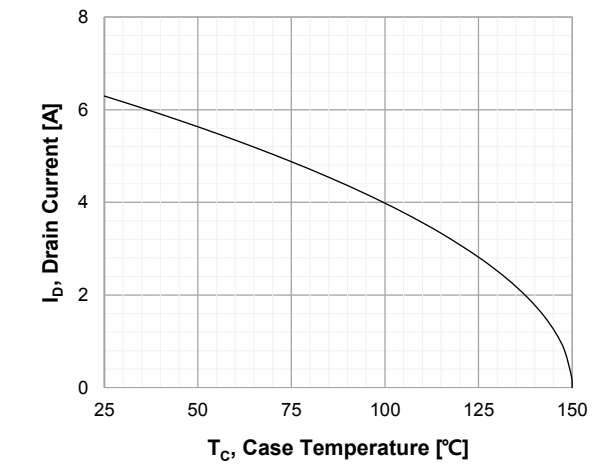


Figure 11. E_{oss} vs. Drain to Source Voltage

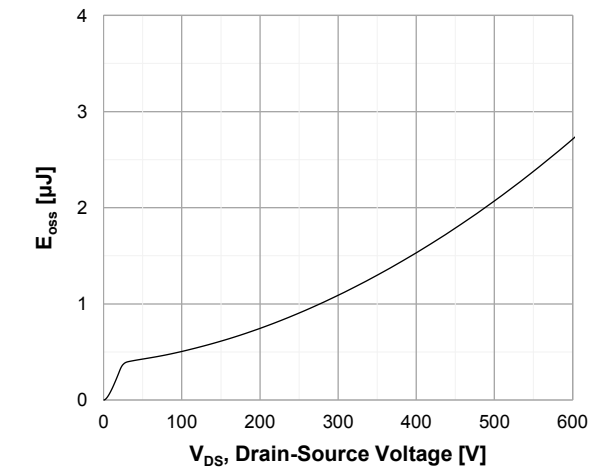
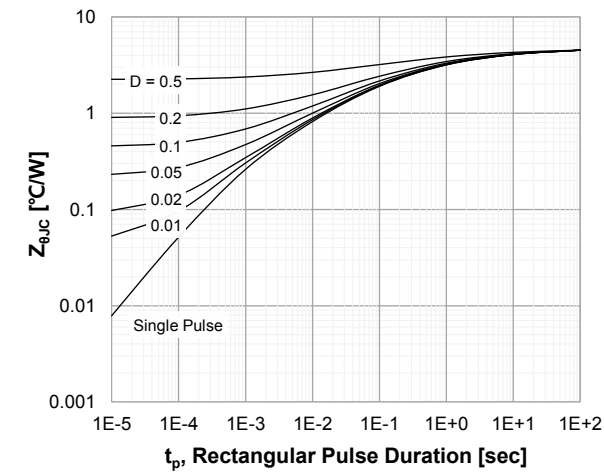


Figure 12. Transient Thermal Response Curve



Test Circuits

Figure 13. Inductive Load Switching Test Circuit and Waveforms

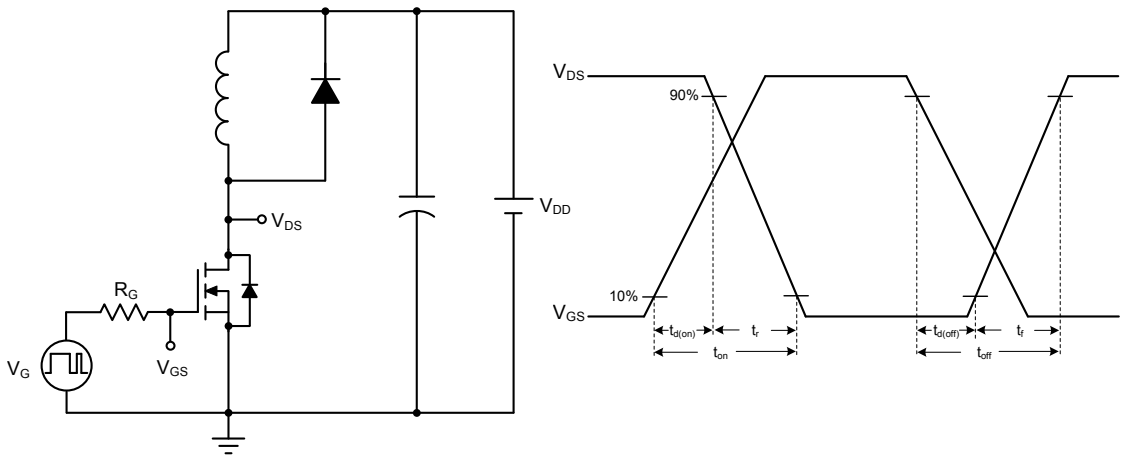


Figure 14. Unclamped Inductive Switching Test Circuit and Waveforms

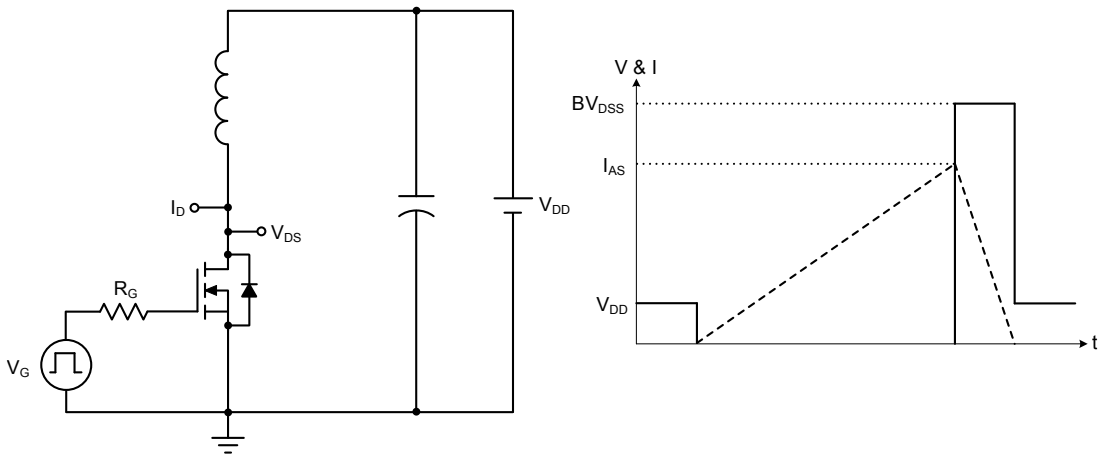
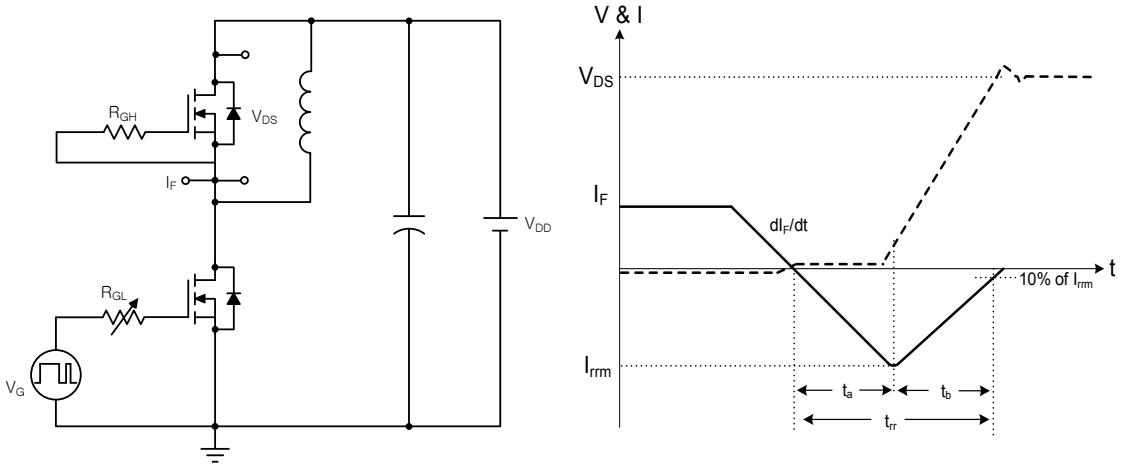


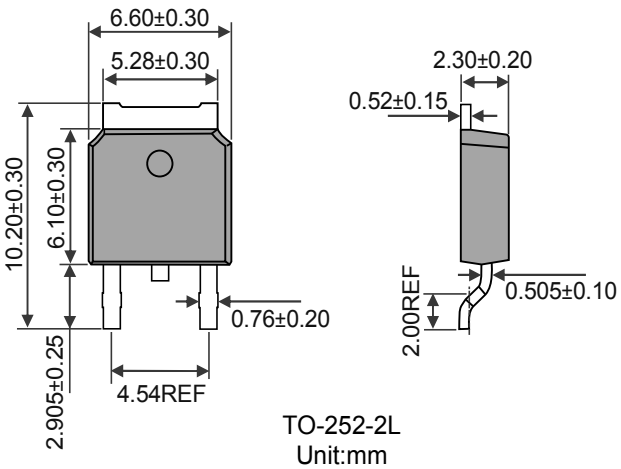
Figure 15. Peak Diode Recovery dv/dt Test Circuit and Waveforms



Package Outlines

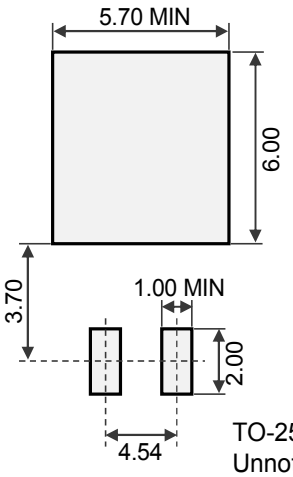
TO-252-2L

Package Outline Dimensions



TO-252-2L
Unit:mm

Suggested Solder Pad Layout



TO-252-2L
Unnoted Tolerance:±0.05
Unit:mm

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