



## 600V N-ch Multi-Epi Super-Junction MOSFET

**Pb** Lead Free Package and Finish

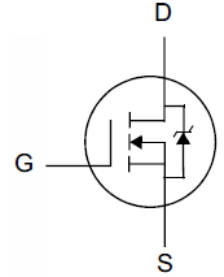
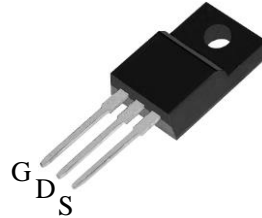
### General Features

- Proprietary New Super-Junction Technology
- $R_{DS(ON),typ.}=110m\Omega@V_{GS}=10V$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

$BV_{DSS}$	$R_{DS(ON),typ.}$	$I_D$
600V	110m $\Omega$	25A

### Applications

- Adaptor
- Charger
- SMPS Standby Power
- Switching Voltage Regulators



TO-220F

Package Not to Scale

### Ordering Information

Part Number	Package	Brand
SPTA60R130FD	TO-220F	

### Absolute Maximum Ratings

$T_C=25^{\circ}C$  unless otherwise specified

Symbol	Parameter	Value	Unit
		SPTA60R130FD	
$V_{DSS}$	Drain-to-Source Voltage	600	V
$V_{GSS}$	Gate source voltage (static)	$\pm 30$	
$I_D$	Continuous Drain Current @ $T_C = 25^{\circ}C$	25	A
	Continuous Drain Current @ $T_C = 100^{\circ}C$	16	
$I_{DM}$	Pulsed Drain Current at $V_{GS}=10V$	75	
$E_{AS}$	Single Pulse Avalanche Energy	786	mJ
$P_D$	Power Dissipation	32	W
$T_J \& T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^{\circ}C$

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

### Thermal Characteristics

Symbol	Parameter	Max. Value	Unit
		SPTA60R130FD	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.92	$^{\circ}C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	80	



## Electrical Characteristics

### OFF Characteristics

$T_J = 25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	600	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	10	$\mu A$	$V_{DS}=600V, V_{GS}=0V$
		--	--	100		$V_{DS}=480V, V_{GS}=0V, T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Leakage Current	--	--	+100	nA	$V_{GS}=+30V, V_{DS}=0V$
		--	--	-100		$V_{GS}=-30V, V_{DS}=0V$

### ON Characteristics

$T_J = 25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	110	130	m $\Omega$	$V_{GS}=10V, I_D=10A$
$V_{GS(TH)}$	Gate Threshold Voltage	2.5	3.5	4.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$

### Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$C_{iss}$	Input Capacitance	--	1955	--	$\mu F$	$V_{GS}=0V, V_{DS}=50V, f=1.0MHz$
$C_{oss}$	Output Capacitance	--	170	--		
$C_{rSS}$	Reverse Transfer Capacitance	--	1.3	--		
$Q_g$	Total Gate Charge	--	41.3	--	nC	$V_{DD}=480V, I_D=25A, V_{GS}=0 \text{ to } 10V$
$Q_{gs}$	Gate-to-Source Charge	--	10.9	--		
$Q_{gd}$	Gate-to-Drain (Miller) Charge	--	16.5	--		

### Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	56	--	ns	$V_{DD}=300V, I_D=25A, V_{GS}=10V, R_g=25\Omega$
$t_{rise}$	Rise Time	--	194	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	80	--		
$t_{fall}$	Fall Time	--	69	--		

**Source-Drain Body Diode Characteristics**T<sub>J</sub>=25°C unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I <sub>SD</sub>	Continuous Source Current <sup>[2]</sup>	--	--	25	A	Maximum Ratings
I <sub>SM</sub>	Pulsed Source Current <sup>[2]</sup>	--	--	75		
V <sub>SD</sub>	Diode Forward Voltage	--	--	1.2	V	I <sub>S</sub> =12.5A, V <sub>GS</sub> =0V
T <sub>rr</sub>	Reverse Recovery Time	--	184	--	nS	I <sub>S</sub> =25A , di/dt =100A/us
Q <sub>rr</sub>	Reverse Recovery Charge	--	0.98	--	uC	

**Note:**[1] T<sub>J</sub>=+25°C to +150°C

[2] Pulse width≤380μs; duty cycle≤2%.



### Typical Characteristics:

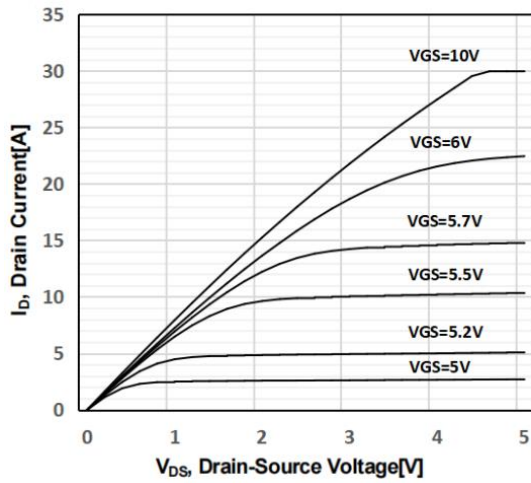


Figure 1. Output Characteristics

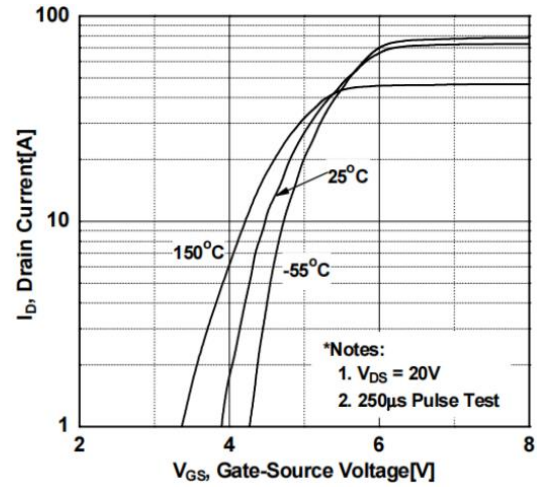


Figure 2. Transfer Characteristics

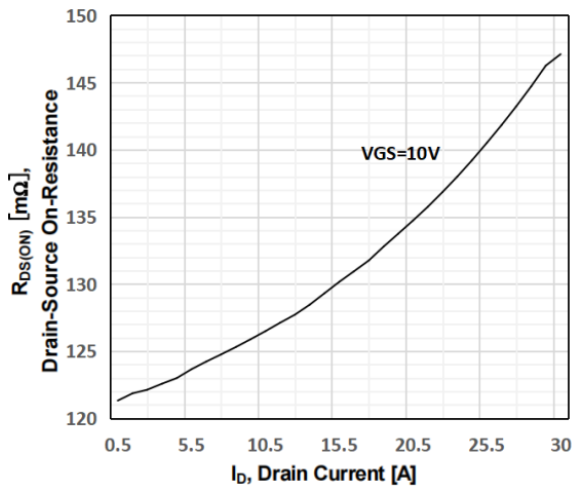


Figure 3. On-Resistance vs. Drain Current

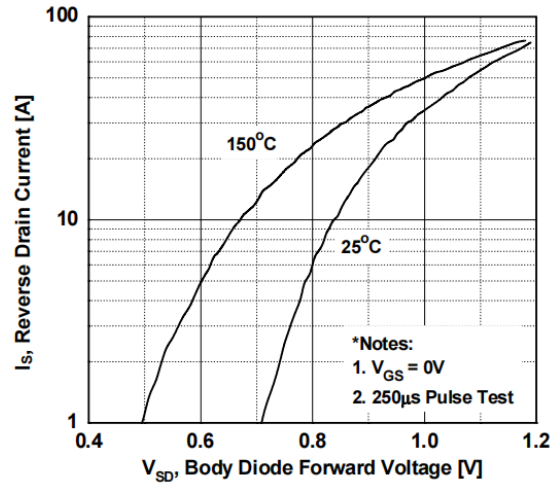


Figure 4. Body Diode Forward Voltage

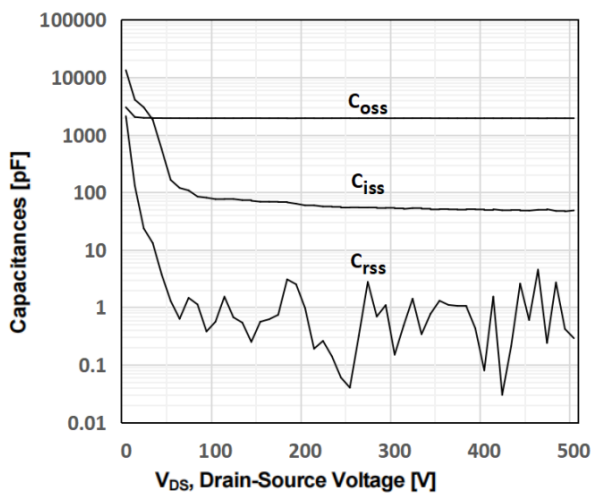


Figure 5. Capacitance

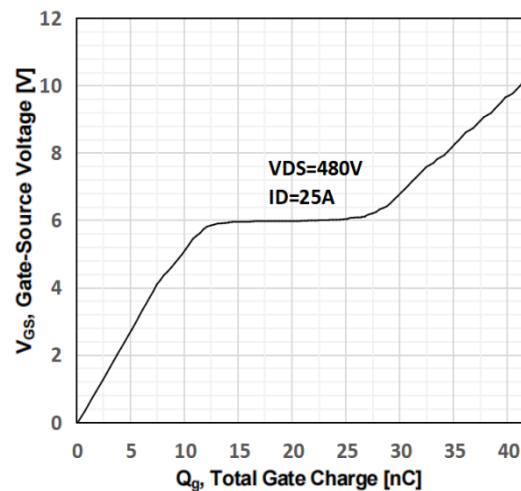


Figure 6. Gate Charge



### Typical Characteristics:

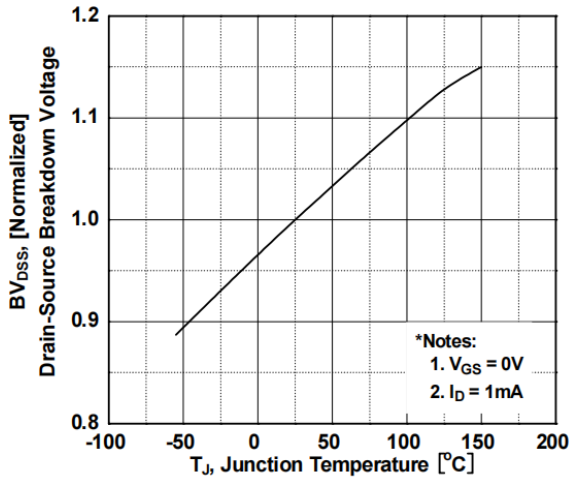


Figure 7. Breakdown Voltage vs. Temperature

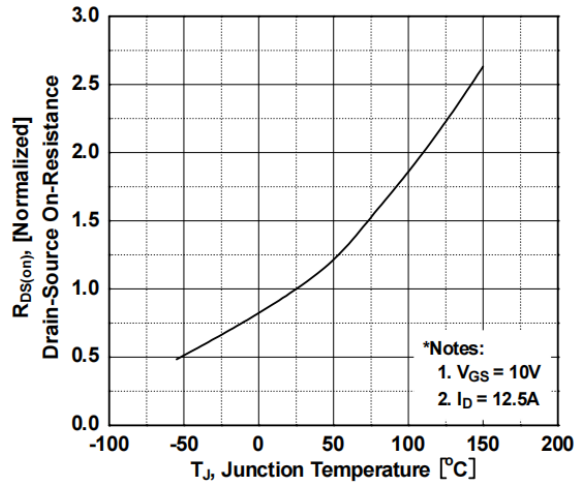


Figure 8. On-Resistance vs. Temperature

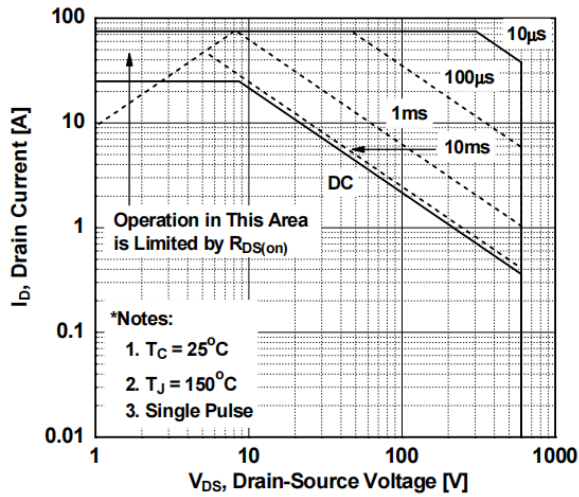


Figure 9. Maximum Forward Bias Safe Operating Area

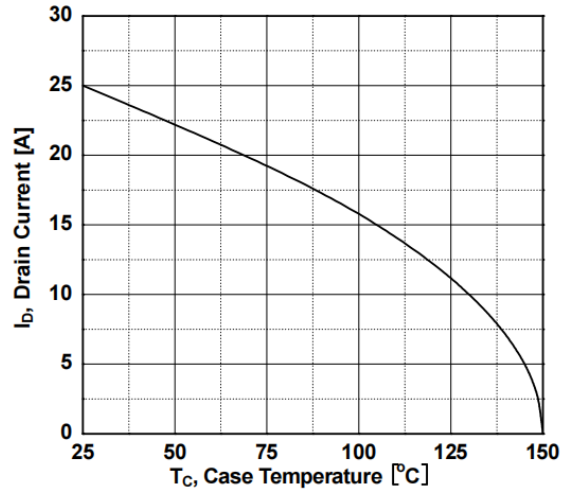


Figure 10. Maximum Continuous Drain Current vs. Temperature

Test Circuits and Waveforms

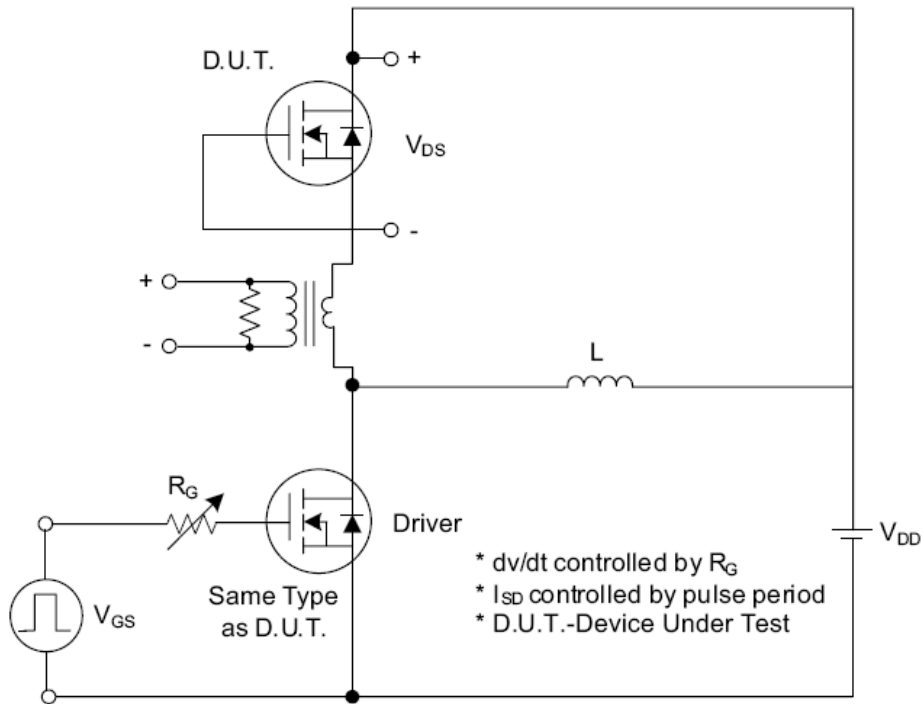


Fig. 1.1 Peak Diode Recovery  $dv/dt$  Test Circuit

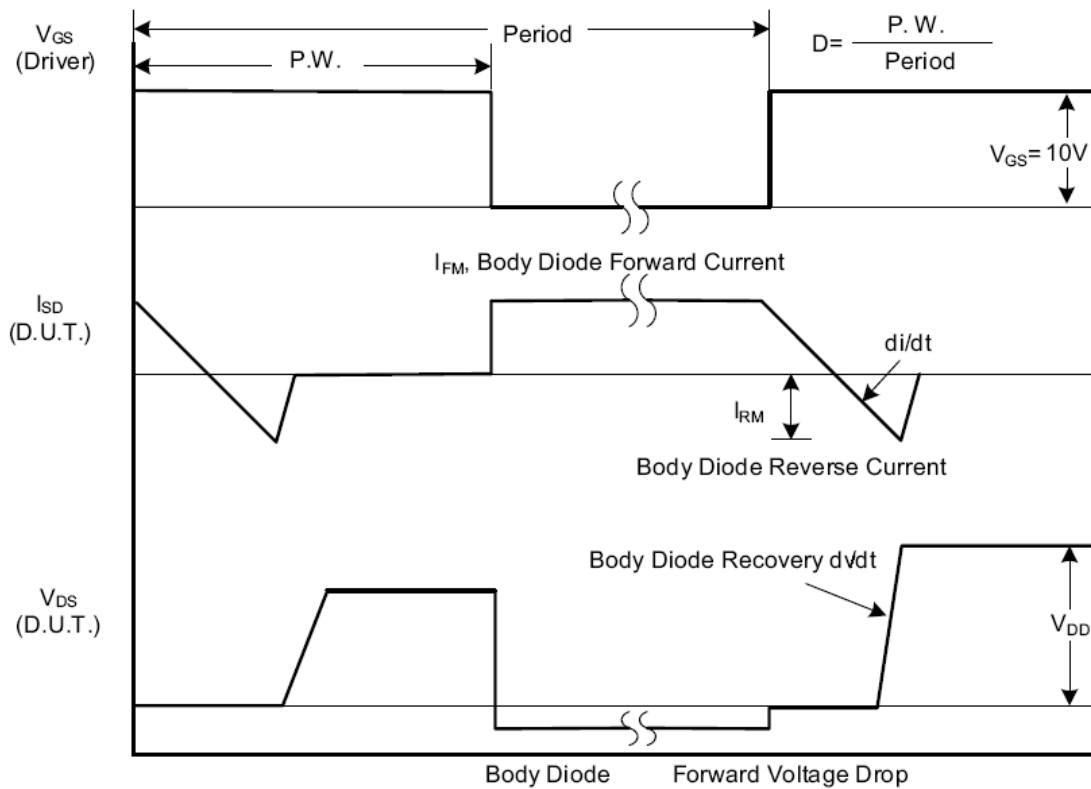


Fig. 1.2 Peak Diode Recovery  $dv/dt$  Waveforms

Test Circuits and Waveforms (Cont.)

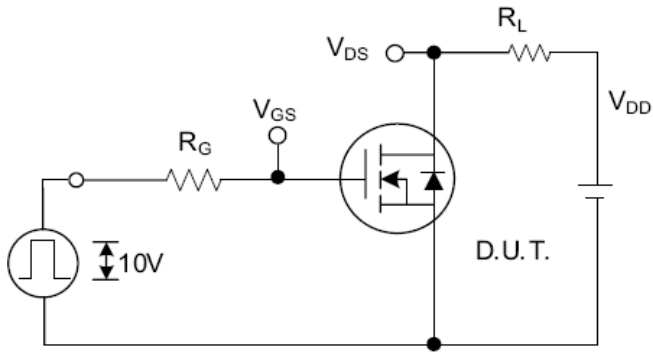


Fig. 2.1 Switching Test Circuit

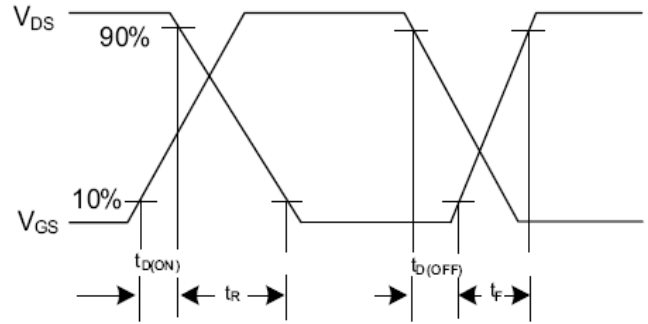


Fig. 2.2 Switching Waveforms

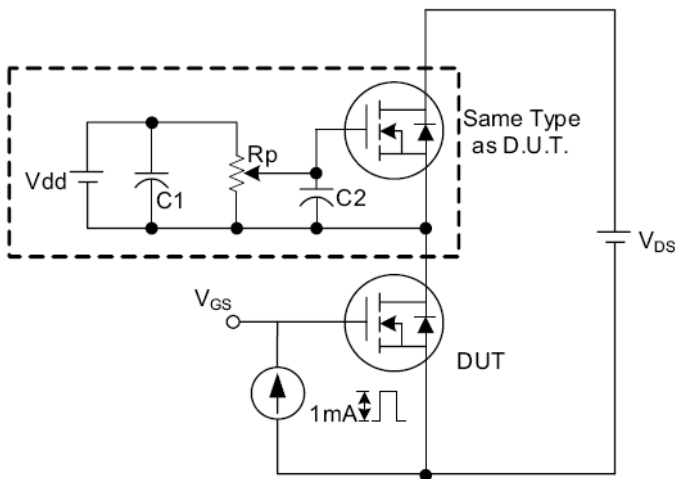


Fig. 3.1 Gate Charge Test Circuit

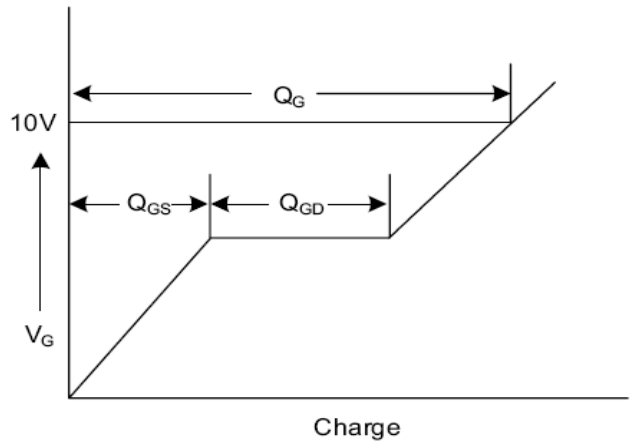


Fig. 3.2 Gate Charge Waveform

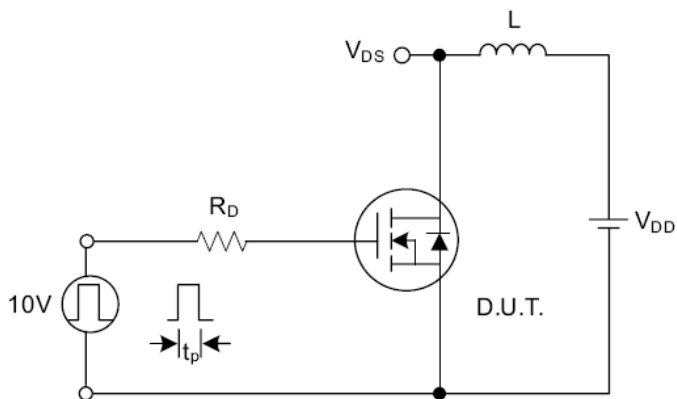


Fig. 4.1 Unclamped Inductive Switching Test Circuit

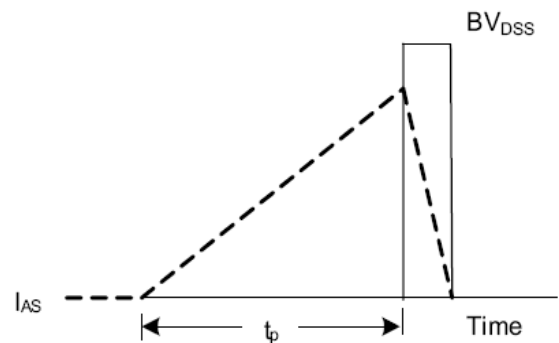


Fig. 4.2 Unclamped Inductive Switching Waveforms



---

## Disclaimers:

Perfect Intelligent Power Semiconductor Co., Ltd (PIP) reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information is current and complete. All products are sold subject to PIP's terms and conditions supplied at the time of order acknowledgement.

Perfect Intelligent Power Semiconductor Co., Ltd warrants performance of its hardware products to the specifications at the time of sale, Testing, reliability and quality control are used to the extent PIP deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

Perfect Intelligent Power Semiconductor Co., Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using PIP's components. To minimize risk, customers must provide adequate design and operating safeguards.

Perfect Intelligent Power Semiconductor Co., Ltd does not warrant or convey any license either expressed or implied under its patent rights, nor the rights of others. Reproduction of information in PIP's data sheets or data books is permissible only if reproduction is without modification or alteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. Perfect Intelligent Power Semiconductor Co., Ltd is not responsible or liable for such altered documentation.

Resale of PIP's products with statements different from or beyond the parameters stated by Perfect Intelligent Power Semiconductor Co., Ltd for that product or service voids all express or implied warranties for the associated PIP's product or service and is unfair and deceptive business practice. Perfect Intelligent Power Semiconductor Co., Ltd is not responsible or liable for any such statements.

---

## Life Support Policy:

Perfect Intelligent Power Semiconductor Co., Ltd's products are not authorized for use as critical components in life support devices or systems without the expressed written approval of Perfect Intelligent Power Semiconductor Co., Ltd.

As used herein:

1. Life support devices or systems are devices or systems which:
  - a. are intended for surgical implant into the human body,
  - b. support or sustain life,
  - c. whose failure to perform when properly used in accordance with instructions for used provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.