



250V N-Channel MOSFET

Lead Free Package and Finish

General Features

- Proprietary New Trench Technology
- $R_{DS(ON),typ.} = 85\text{ m}\Omega @ V_{GS}=10\text{V}$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

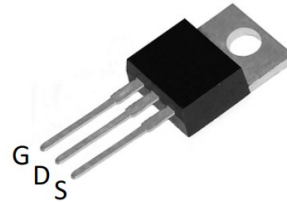
Applications

- Synchronous Rectification in SMPS
- Motor Control
- Hard Switching and High Speed Circuit

Ordering Information

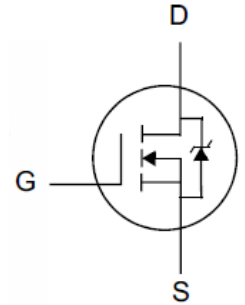
Part Number	Package	Brand
SPTP25R80KA	TO-220	

BV_{DSS}	$R_{DS(ON),typ.}$	I_D
250V	85m Ω	20A



TO-220

Package No to Scale



Absolute Maximum Ratings

$T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Limit	Unit
V_{DSS}	Drain-to-Source Voltage ^[1]	250	V
V_{GSS}	Gate-to-Source Voltage	± 20	
I_D	Continuous Drain Current	20	A
	Continuous Drain Current @ $T_C=100^\circ\text{C}$	14	
I_{DM}	Pulsed Drain Current at $V_{GS}=10\text{V}$ ^[2]	70	
E_{AS}	Single Pulse Avalanche Energy $L=1\text{mH}$	180	mJ
P_D	Power Dissipation	125	W
	Derating Factor above 25°C	0.83	W/ $^\circ\text{C}$
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300	$^\circ\text{C}$
		260	
$T_J \& T_{STG}$	Operating and Storage Temperature Range	-55 to 175	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Limit	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	



Electrical Characteristics

OFF Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	--	--	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	$V_{DS}=250V, V_{GS}=0V$
		--	--	100		$V_{DS}=200V, V_{GS}=0V, T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	$V_{GS}=+20V, V_{DS}=0V$
		--	--	-100		$V_{GS}=-20V, V_{DS}=0V$

ON Characteristics

 $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance ^[3]	--	85	100	$m\Omega$	$V_{GS}=10V, I_D=10A$
$V_{GS(TH)}$	Gate Threshold Voltage	2.5	--	4.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	1477	--	pF	$V_{GS}=0V, V_{DS}=125V, f=1.0MHz$
C_{rSS}	Reverse Transfer Capacitance	--	12	--		
C_{oss}	Output Capacitance	--	72.5	--		
Q_g	Total Gate Charge	--	19	--	nC	$V_{DD}=125V, I_D=10A, V_{GS}=10V$
Q_{gs}	Gate-to-Source Charge	--	7	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	3.9	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	16.8	--	ns	$V_{DD}=125V, I_D=10A, V_{GS}=10V, R_G=2.35\Omega$
t_{rise}	Rise Time	--	4	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	23.6	--		
t_{fall}	Fall Time	--	4.4	--		



Source-Drain Body Diode Characteristics

$T_J=25^{\circ}\text{C}$ unless otherwise specified

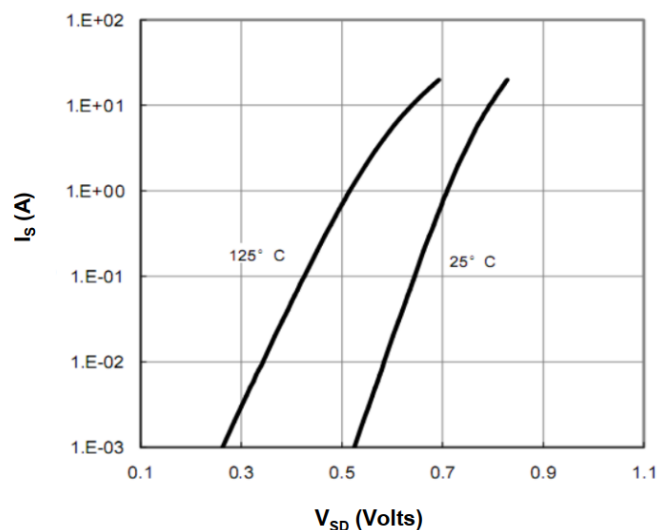
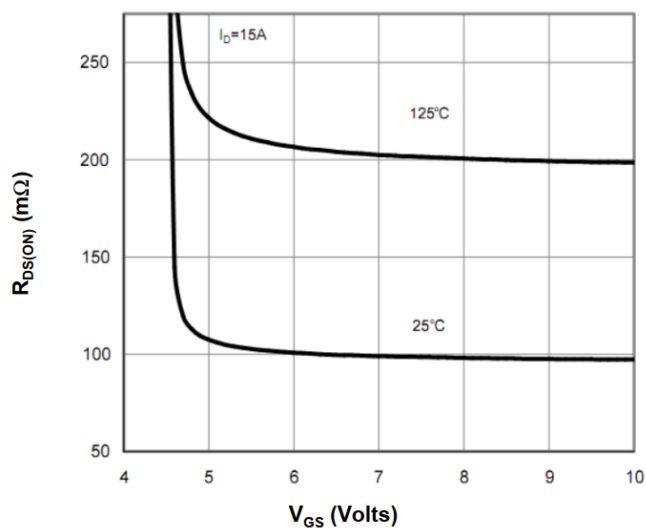
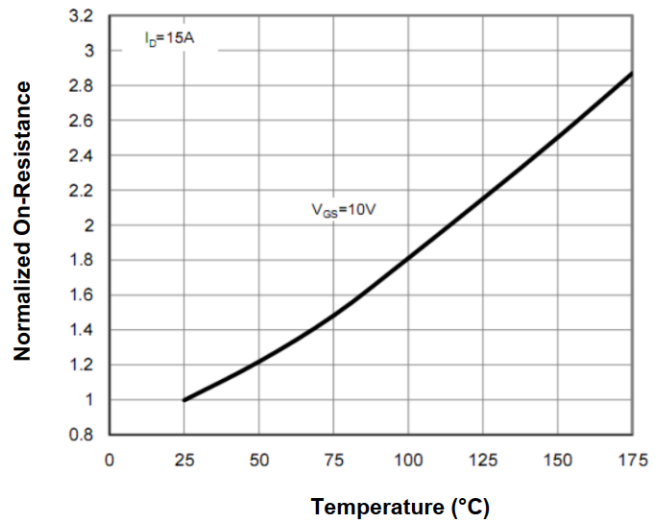
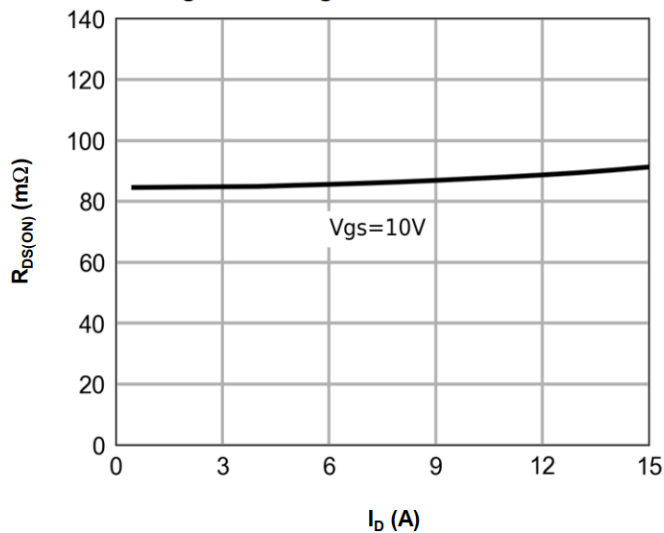
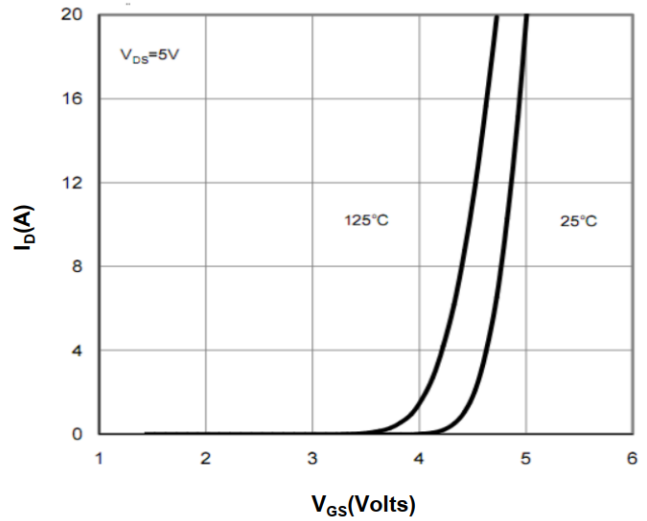
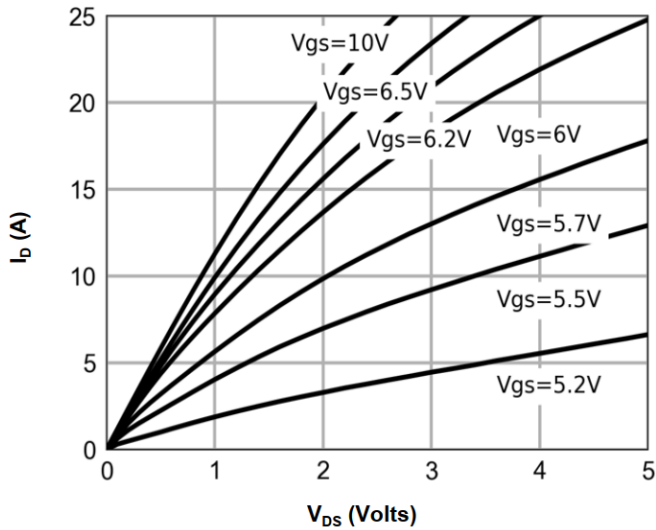
Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current	--	--	20	A	Integral PN-diode in MOSFET
I_{SM}	Pulsed Source Current	--	--	70		
V_{SD}	Diode Forward Voltage	--	--	1.2	V	$I_S=20\text{A}$, $V_{GS}=0\text{V}$
t_{rr}	Reverse recovery time	--	162	--	ns	$I_F=10\text{A}$, $di_F/dt=100\text{A}/\mu\text{s}$
Q_{rr}	Reverse recovery charge	--	515	--	nC	

Note:

- [1] $T_J=+25^{\circ}\text{C}$ to $+175^{\circ}\text{C}$.
- [2] Repetitive rating; pulse width limited by maximum junction temperature.
- [3] Pulse width $\leq 380\mu\text{s}$; duty cycle $\leq 2\%$.



Typical Characteristics



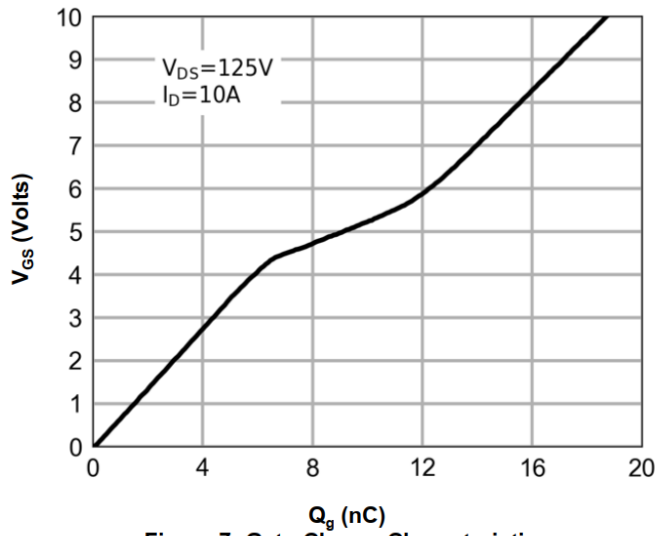


Figure 7: Gate-Charge Characteristics

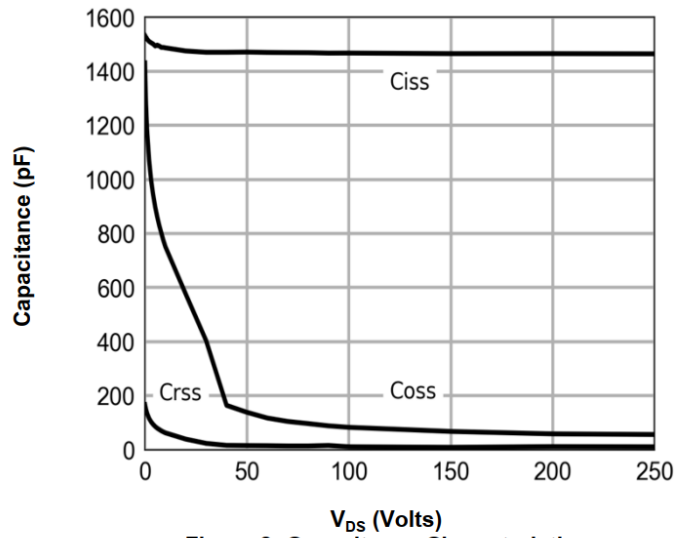


Figure 8: Capacitance Characteristics

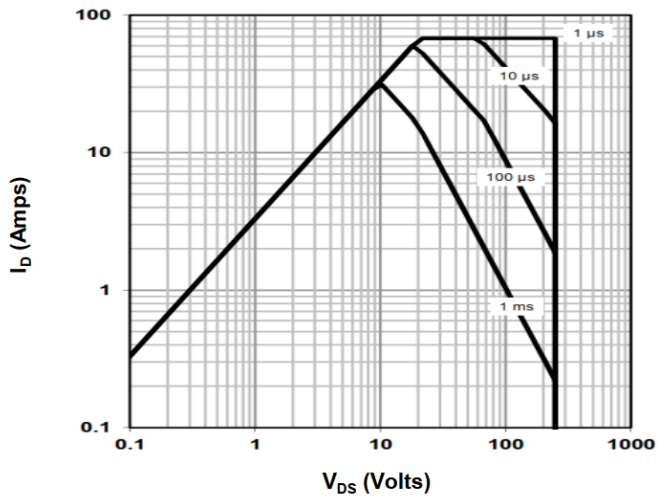


Figure 9: Maximum Forward Biased Safe Operating Area

Test Circuits and Waveforms

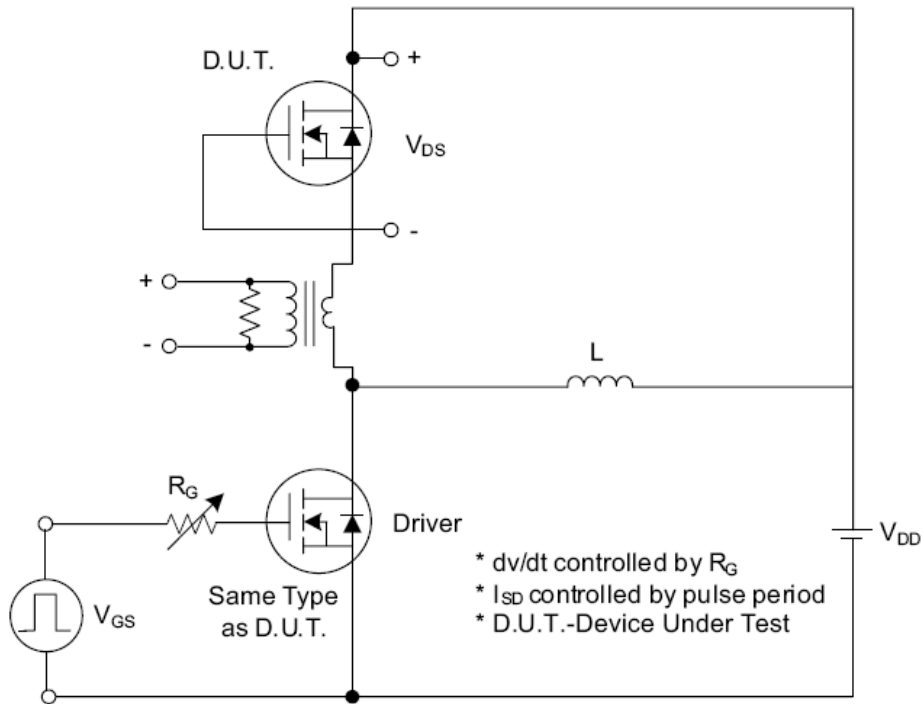


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

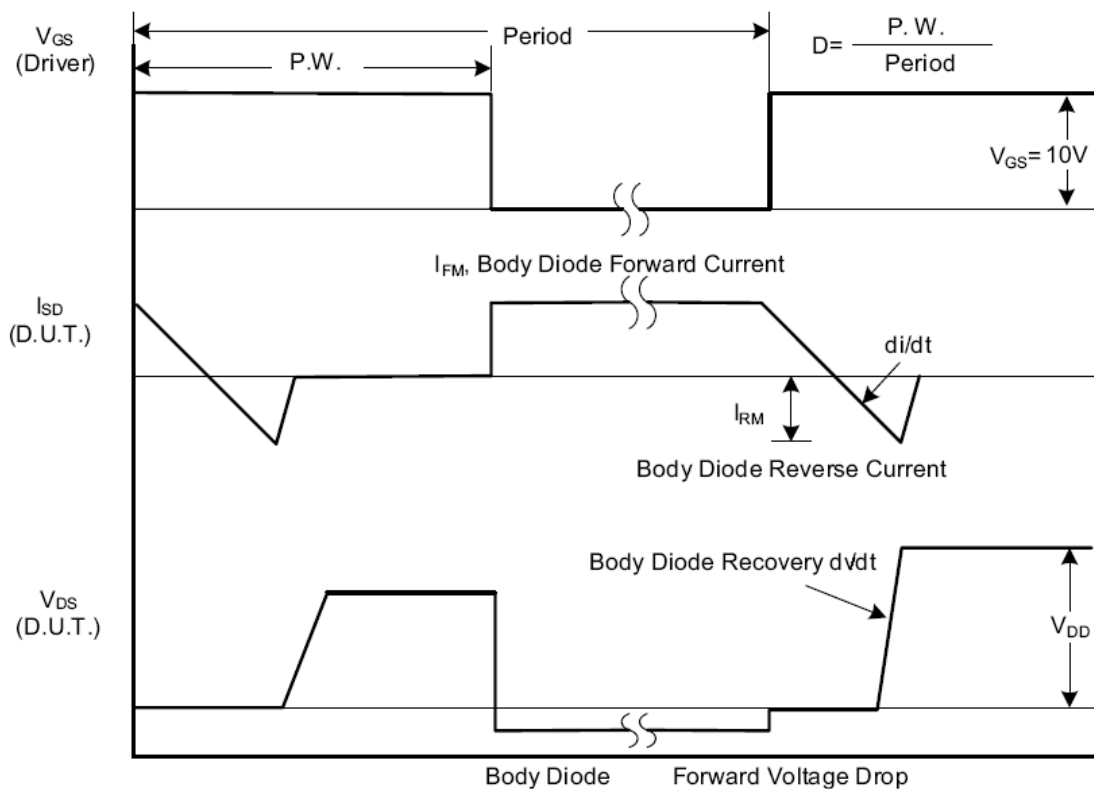


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

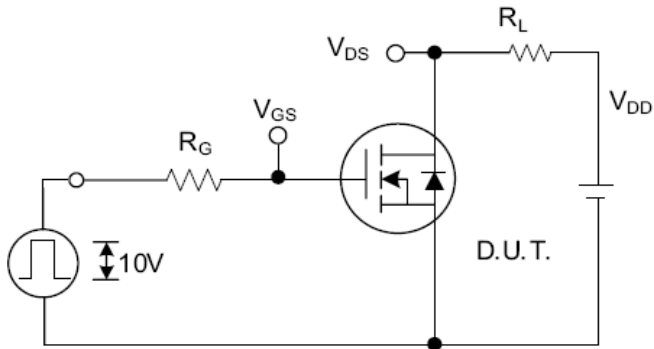


Fig. 2.1 Switching Test Circuit

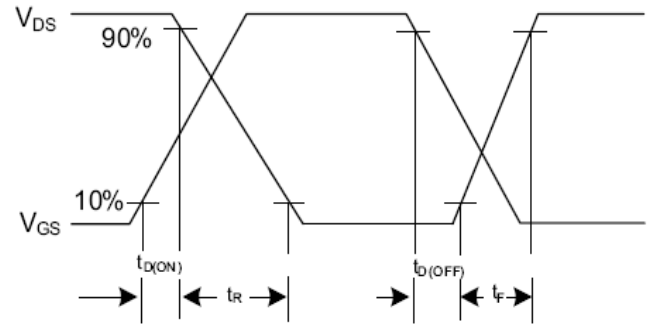


Fig. 2.2 Switching Waveforms

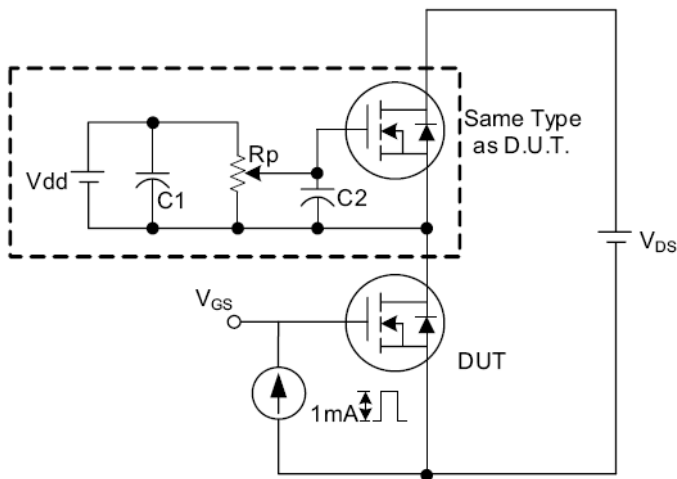


Fig. 3.1 Gate Charge Test Circuit

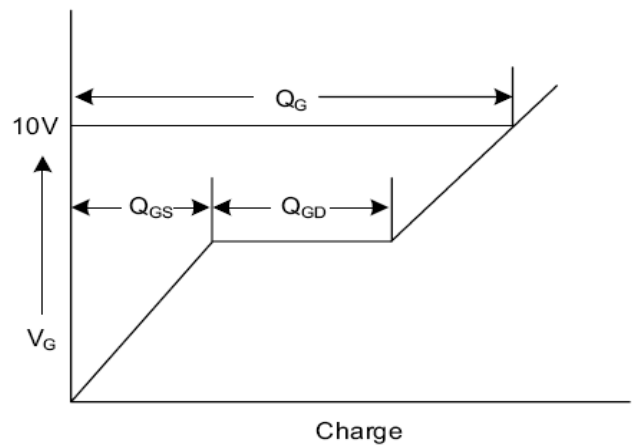


Fig. 3.2 Gate Charge Waveform

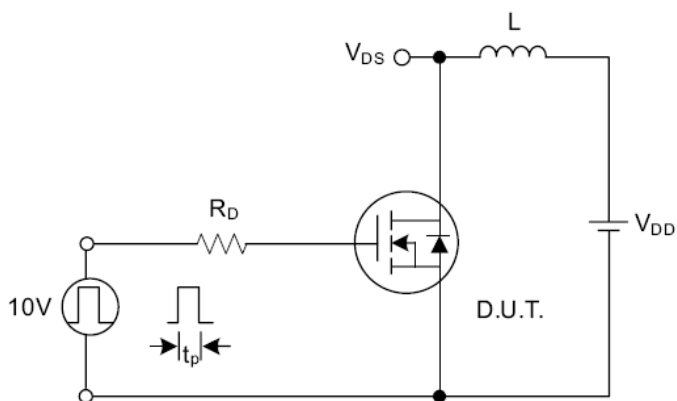


Fig. 4.1 Unclamped Inductive Switching Test Circuit

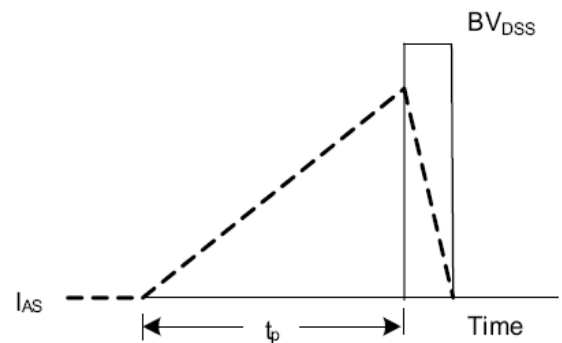


Fig. 4.2 Unclamped Inductive Switching Waveforms



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